

ABSTRACT OF THE DISCLOSURE

A Media Access Control (MAC) Bus interface definition and multiplexor scheme that may be implemented to provide chip layout-insensitive connections between a number of communication physical layer port entities and a single buffer manager or communications controller entity, utilizing a set of independent pipelined buses. The interface comprising three buses: A MAC In Data bus, a MAC Out Data bus, and a MAC Out Message bus. Each bus can operated with an independent set of timing signals to enable data transfers between a system side block and one or more network side blocks. The multiplexor scheme provides a multiplexor for each of the MAC buses, and enables a single system side block to connect to multiple network side blocks. The multiplexors may be also be cascaded.